Amendment to the Claims:

The following listing of claims replaces all previous versions and listings of claims:

1. (Currently Amended) A system for memory management, the system comprising a tag cache in communication with one or more cache devices in a storage hierarchy, wherein:

the tag cache includes tags of recently accessed memory blocks, each tag corresponding to one of the memory blocks and each tag including tag contents; wherein the tag contents include a memory block real address and one bit for every memory line in the memory block, said bits referred to as prefetch bits; and wherein further, each of the prefetch bits is reset to a non-prefetch status with a selected probability of between zero and one;

the tag contents control which memory lines of the corresponding memory block are prefetched into at least one of the cache devices;

the tag contents are updated using a selected subset of processor references, said subset referred to as filtered references; and

the tag contents are modified probabilistically at selected times or events.

2. (Cancelled)

3. (Cancelled)

4. (Currently Amended) The system of claim 1 [3] wherein the tag contents further include a bit to control prefetching of memory lines from a next virtual memory block, said bit referred to as a next virtual memory block bit.

5. (Original) The system of claim 4 wherein the next virtual memory block bit in a preceding memory block in a virtual address space is set to a prefetch status when the preceding memory block tag is in the tag cache.

6. (Original) The system of claim 4 wherein the next virtual memory block bit is

turned to a nonprefetch status with a specified probability on certain events.

7. (Original) The system of claim 6 wherein the certain events include eviction of the tag from the tag cache.

8. (Currently Amended) The system of claim 1 [3] wherein:

one of the cache devices is a level two cache device and another is a level one cache device;

the prefetch bits are set by a selected subset of misses from the level one cache device; and

the misses include at least one miss from the level two cache device.

9. (Currently Amended) The method of claim 1 [3] wherein the tag contents include 32 prefetch bits.

10. (Currently Amended) The system of claim 1 [3] wherein the value of each prefetch bit determines whether the corresponding memory line should be prefetched.

11. (Cancelled)

12. (Currently Amended) The system of claim 1 [11] wherein the selected probability is one eighth.

13-21. (Cancelled)

22. (Currently Amended) A method for memory management, the method comprising:

receiving a notification of a cache fault from a cache device, the notification including a fault memory block and a fault memory line;

determining if a tag corresponding to the fault memory block is present in a tag cache, wherein the tag includes prefetch bits corresponding to memory lines contained in a memory

block specified by the tag;

in response to not locating the tag corresponding to the fault memory block in the tag cache:

fetching the tag corresponding to the fault memory block into the tag cache;

prefetching the memory lines corresponding to the prefetch bits in the tag that are set to a prefetch status, said prefetching into the cache device; and

resetting each of the prefetch bits which were set to a prefetch status to a nonprefetch status with a selected probability, wherein the selected probability is one eighth; and

setting the prefetch bit corresponding to the fault memory line in the tag to the prefetch status.

23-32. (Cancelled)